A clean copy of the title and paragraph in the specification affected by the present Amendment appear in the Appendix hereto.

Request for Rejoinder

Applicants solicit rejoinder of nonelected method claims 1 through 6, upon the determination of an allowable device claim, pursuant to the provisions of MPEP§821.04.

Drawing Objection

The Examiner objected to the drawings pursuant to 37 C.F.R. §1.84(b)(5), asserting that reference characters 101 and 103a in Fig. 16 are not disclosed.

This rejection is traversed. In response, page 1 of the written specification has been amended to identify reference characters 101 and 103a in Fig. 16, thereby overcoming the stated basis for the drawing objection. Accordingly, withdrawal of the drawing objection is solicited.

Objection to the Specification

The Examiner asserted that the title of the invention is not descriptive and required a new title. In response, the title has been changed to --METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE--. Accordingly, withdrawal of the objection to the specification is solicited.

Claims 7 through 11 were rejected under 35 U.S.C. §103 for obviousness predicated upon the acknowledged prior art (Figs. 15 through 17) in view of Hanyu et al.

In the statement of the rejection, the Examiner **admitted** that the acknowledged prior art device does **not** contain a short-circuit preventing insulating film. The Examiner then referred to Fig. 33 of Hanyu et al., lines 49 through 56, and pointed to films 2013a and 2013b asserting they are short-circuit preventing insulating films. The Examiner then concluded that, without actually explaining why, one having ordinary skill in the art would somehow have been motivated to modify the acknowledged prior art semiconductor device by providing a short-circuit preventing insulating film as disclosed by Hanyu et al. with respect to a liquid crystal device. This rejection is traversed as legally erroneous.

Applicants submit that the Examiner did not comply with relevant judicial standards in attempting to establish the requisite motivational element. Specifically, in imposing the rejection under 35 U.S.C. §103, the Examiner must make a "thorough and searching" factual inquiry and, based upon that factual inquiry, explain **why** one having ordinary skill in the art would have been realistically impelled to modify particular prior art, in this case the acknowledged prior art device depicted in Figs. 15 through 17, to arrive at the claimed invention. *In re Lee, 237 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).* That burden has not been discharged.

Specifically, the acknowledged prior art device upon which the Examiner relies upon as a primary reference is a semiconductor device containing word lines and polypads therebetween. On the other hand, the device disclosed by Hanyu et al., which the Examiner

would rely upon as a teaching reference, is a liquid crystal device containing no word lines and polypads therebetween. The Examiner identified film 2013a; however, this film is positioned between an electrode 2012a and an alignment control film 2014a. Short circuit preventing film 2013b is positioned between alignment control 2014b and substrate 2011b with transparent electrode 2012b (Fig. 21). It is not apparent and the Examiner did not explain **why**, repeat **why,** one having ordinary skill in the art would somehow have been realistically impelled to impress a short circuit preventing film between gate structures 103, which already have a protective film 103a thereon, in the acknowledged prior art device. Indeed, the problem addressed and solved by the claimed invention, i.e., short-circuiting by virtue of an opening 9 (Fig. 14) does **not even exist** in the liquid crystal device disclosed by Hanyu et al.

Further, there is a significant structural difference between the claimed invention and the device disclosed by Hanyu et al. Specifically, the short-circuit preventing insulating film 5 of the claimed invention is formed between the plug interconnection and the insulation along the plug interconnection. However, in the device disclosed by Hanyu et al., the short-circuit preventing insulating film 2013a, 2013b, **cover the wires.** This structure is completely different from that of the claimed invention.

It is, therefore, apparent that a prima facie basis to deny patentability to the claimed invention under 35 U.S.C. §103 has not been established for lack of the requisite motivational element. Applicants, therefore, submit that the imposed rejection of claims 7 through 11 under 35 U.S.C. §103 for obviousness predicated upon the acknowledged prior

art (Figs. 15 through 17) in view of Hanyu et al. is not factually or legally viable and, hence, solicit withdrawal thereof.

It should, therefore, be apparent that the objections and rejections of record has been overcome. Applicants then solicit rejoinder of nonelected method claims 1 through 6. Applicants submit that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX

IN THE TITLE:

The new title reads as follows: --METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE--

IN THE SPECIFICATION:

The paragraph on page 1 commencing at line 20 now reads as follows:

When there is a gap of a high aspect ratio between transfer gates as described above, at the time of forming an insulating layer, the gap between the transfer gates cannot be perfectly buried by the insulating layer. A void which extends long in the longitudinal direction of the transfer gate in a plan view often occurs in the insulating layer. Fig. 15 is a plan view showing arrangement of transfer gates and polypads in a DRAM (Dynamic Random Access Memory). Fig. 16 is a cross section taken along line XVI-XVI of Fig. 15. In Fig. 15, in an insulating interlayer 108 for burying the gap between two transfer gates 103, a region 109a with the high possibility of a void occurrence is extending along the gap. In Fig. 16, reference numeral 101 denotes a semiconductor substrate and reference numeral 103a denotes a nitride protection film. When a void 109 occurs in the region 109a as shown in Fig. 16, polysilicon enters the void at the time of depositing polysilicon for making a polypad, and a short circuit occurs between neighboring polypads 104a and 104b as shown in Fig. 17. In Fig. 17, polysilicon 114 for burying the void is so deposited as to connect the neighboring

polypads 104a and 104b. When such a short circuit occurs, the product yield of manufacturing deteriorates. It might cause a delay in deliveries and the like.